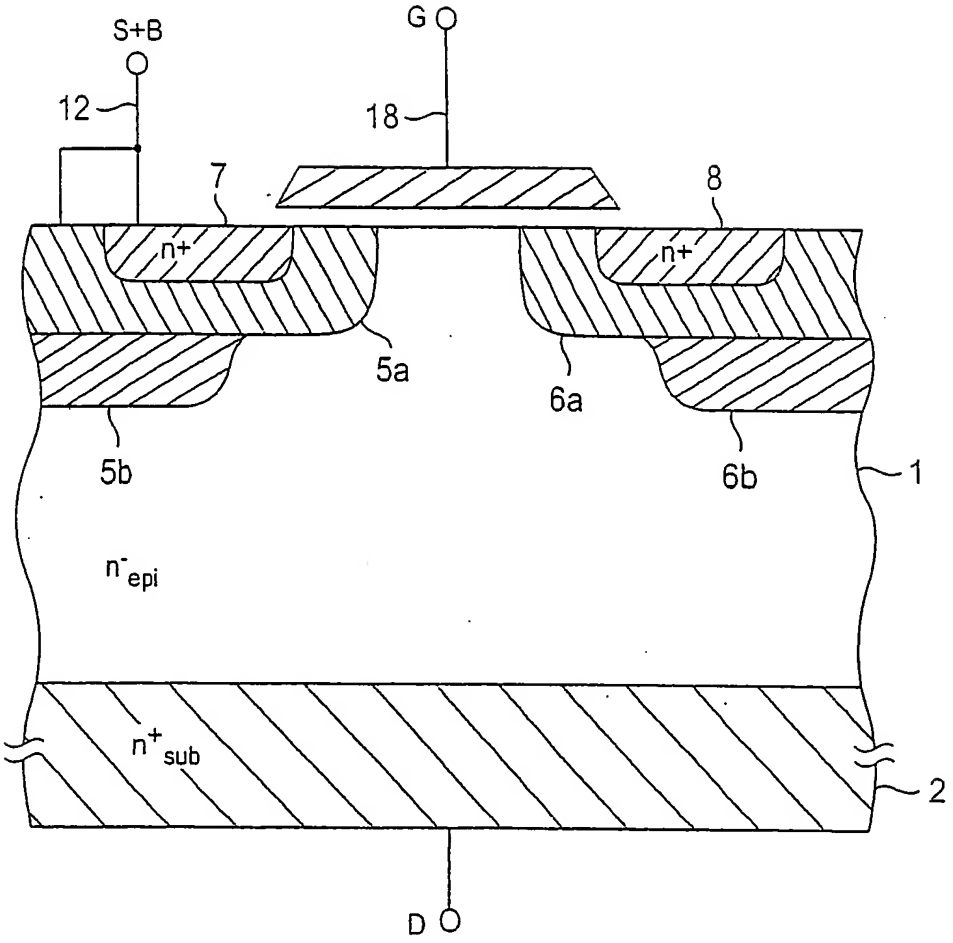


CONVENTIONAL MOSFET

FIG. 1
(PRIOR ART)

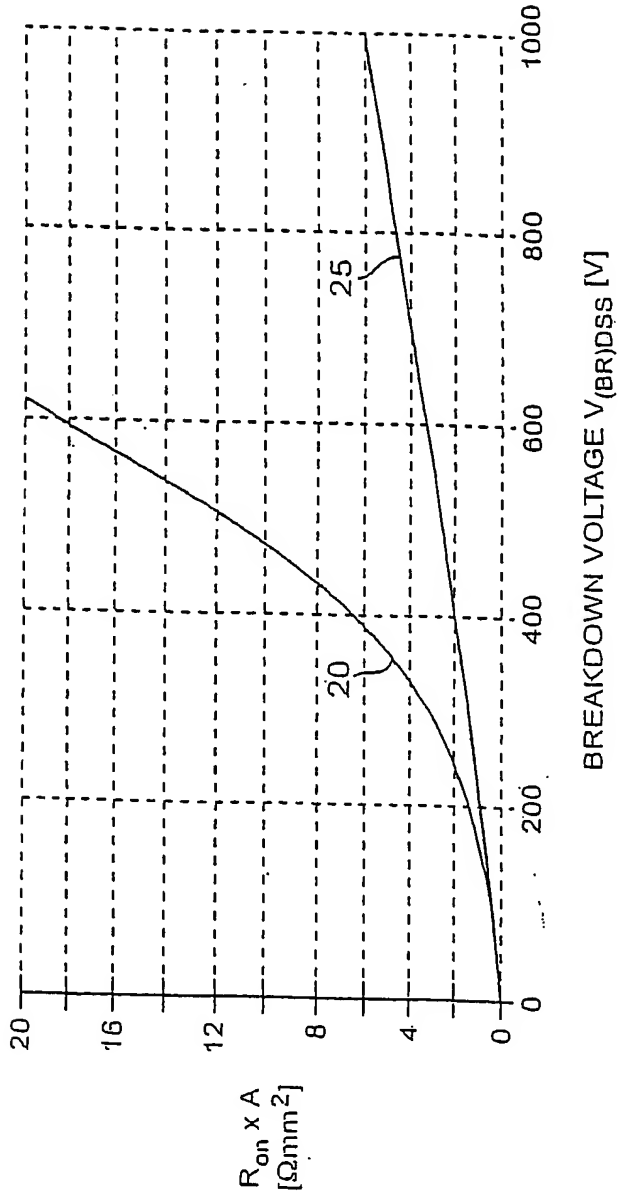
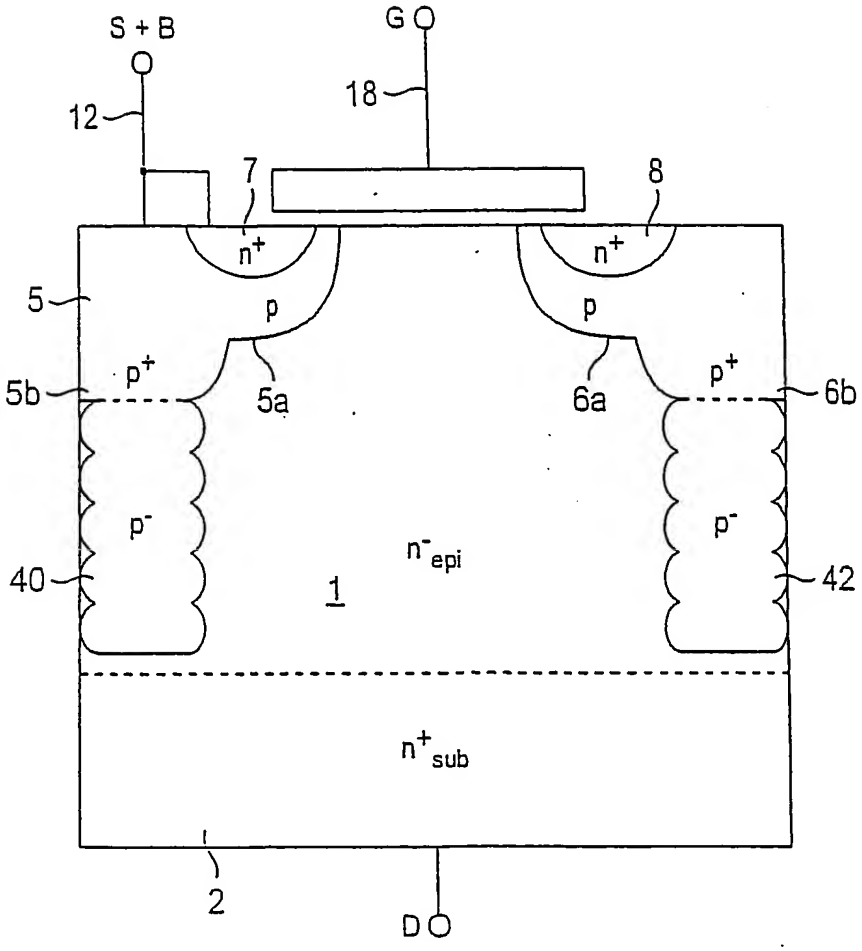

20
16
12
8
4
0
R_{on} x A
[Ωmm²]
0
200
400
600
800
1000
BREAKDOWN VOLTAGE $V_{(BR)DSS}$ [V]
25
20

FIG. 2



THE DOPANT DISTRIBUTION OF A HIGH VOLTAGE VERTICAL DMOS TRANSISTOR WITH A RELATIVELY LOW ON-RESISTANCE

FIG. 3

(PRIOR ART)

1. EPITAXIAL DEPOSITION
2. FORMATION OF THE TRENCH ETCH STOP LAYER
3. MASK AND ETCH THE TRENCH ETCH STOP LAYER
4. TRENCH ETCH

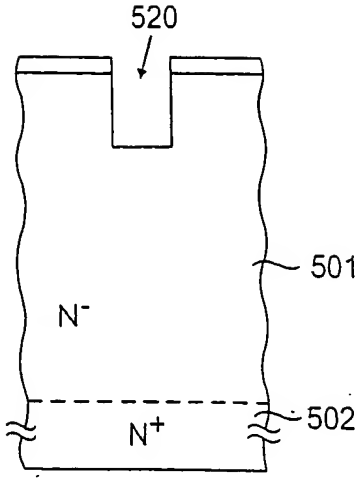


FIG. 4(a)

5. GROW THIN OXIDE LAYER IN THE TRENCH
6. IMPLANT THE DOPANT

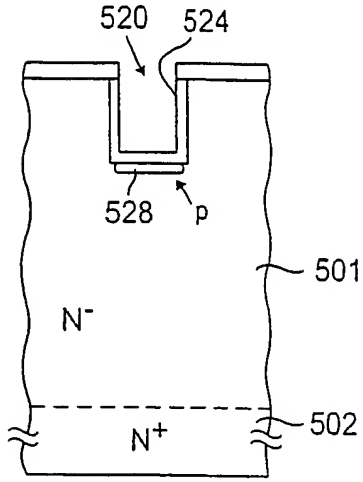


FIG. 4(b)

7. PERFORM A HIGH TEMPERATURE DIFFUSION
8. ETCH THE OXIDE AT THE BOTTOM OF THE TRENCH

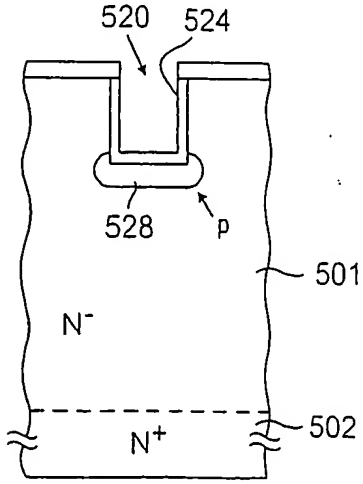


FIG. 4(c)

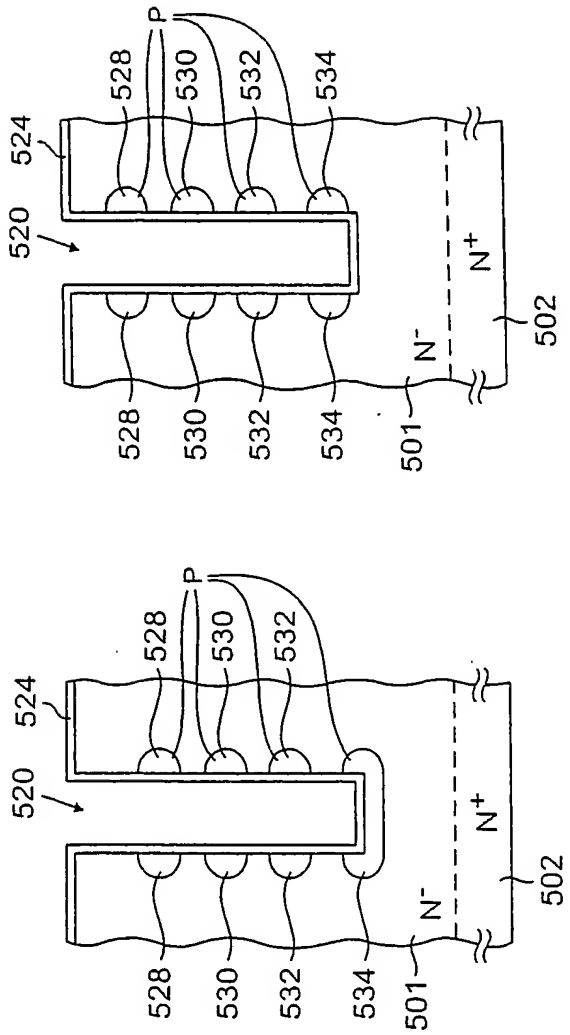


FIG. 4(d)

9. REPEAT THE DOPING AND ETCH STEPS AS MANY TIMES AS REQUIRED

10. DOPE THE REGION FURTHEST FROM THE SURFACE

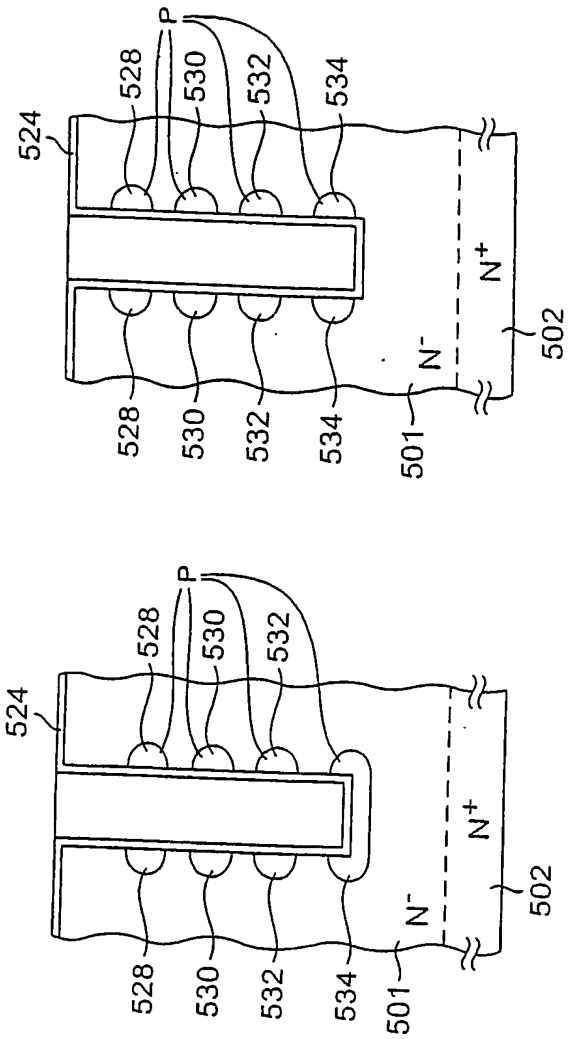

524
528
P
530
532
534
N+
502
N-
501
528
530
532
534
524
528
P
530
532
N+
502
N-
501
528
530
532
534
11. FILL THE TRENCH
12. PLANARIZE THE WAFER SURFACE

FIG. 4(e)

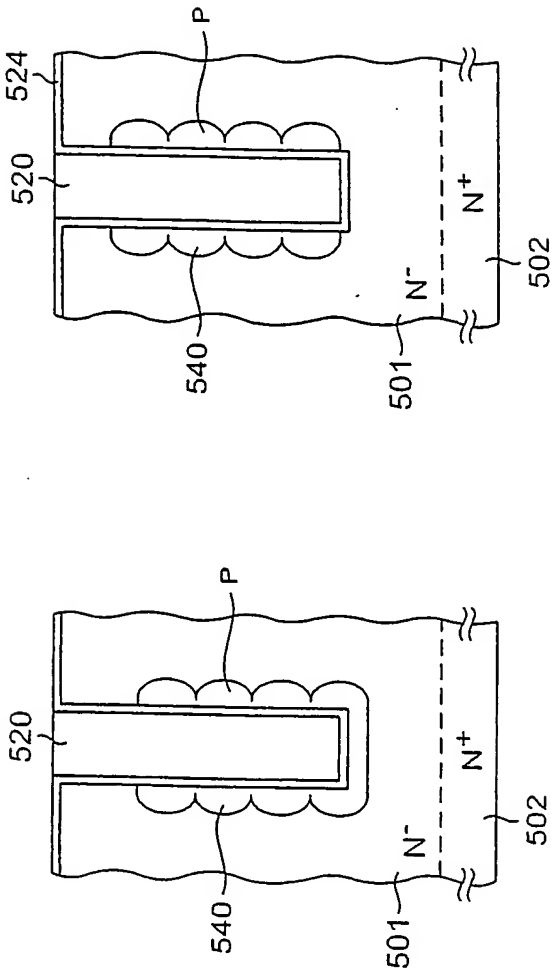


FIG. 4(f)